1. Architecture

8

Reg

4[7:4]

PC

ROM

256x4

8 4[3:0]

IR

MAR

4

Control

Unit

RAM

16x4

Opcode

Mux

A

Buffer

ALU

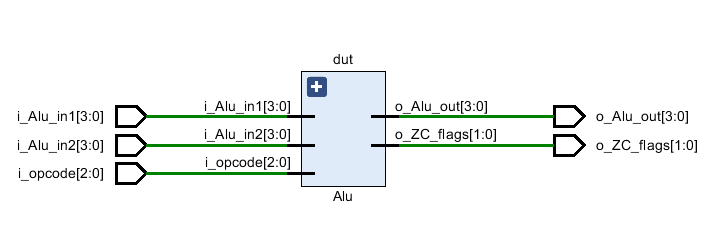
Z C

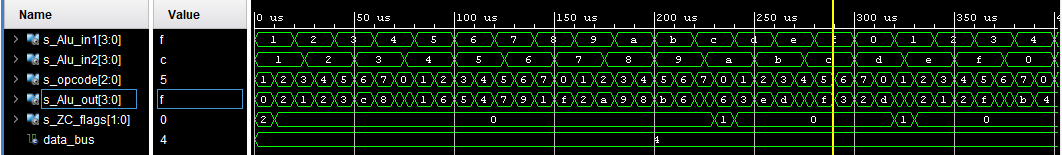
1. Tập lệnh

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Instruction** | **Opcode** | **Instruction Length in bytes** | **Instruction** **Type** | **Operation** | **Comment** |
| **LDA** | 1000 | 1 | MRI | A 🡨 M(addr) | Load register A direct |
| **STA** | 1001 | 1 | MRI | M(addr) 🡨 A | Store register A direct |
| **ADD** | 1010 | 1 | MRI | A 🡨 A + M(addr) | Add register A direct |
| **SUB** | 1011 | 1 | MRI | A 🡨 A – M(addr) | Subtract register A direct |
| **JZ** | 1100 | 1,5 | MRI | If Z = 1 then PC 🡨 (addr) else PC 🡨 PC + 1 | Jum on zero flag set |
| **JC** | 1101 | 1,5 | MRI | If C = 1 then PC 🡨 (addr) else PC 🡨 PC + 1 | Jump on carry flag set |
| **AND** | 1110 | 1 | MRI | A 🡨 A **and** M(addr) | And register A direct |
| **CMA** | 0000 | haft | NMRI | A 🡨 **not** A | Complement register A |
| **INCA** | 0010 | haft | NMRI | A 🡨 A + 1 | Increment register A |
| **DCRA** | 0100 | haft | NMRI | A 🡨 A - 1 | Decrement register A |
| **HLT** | 0110 | haft | NMRI | Halt | Halt CPU |

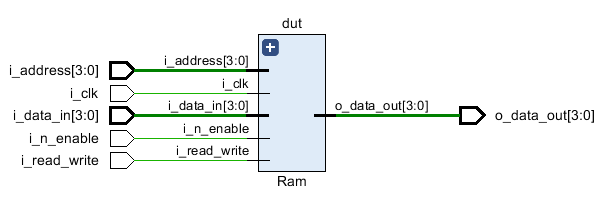
MRI: Memory Reference Instruction, NMRI: Non-Memory Reference Instruction

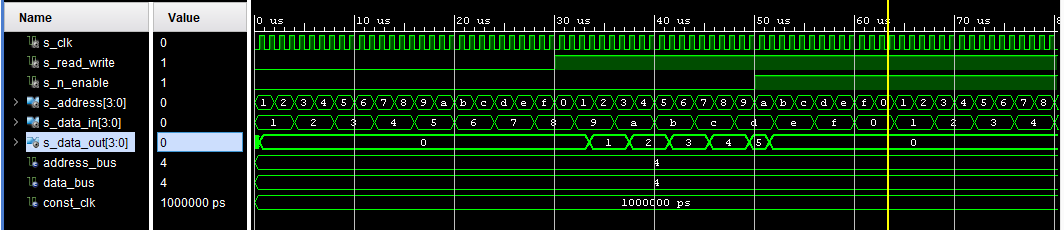
1. Alu



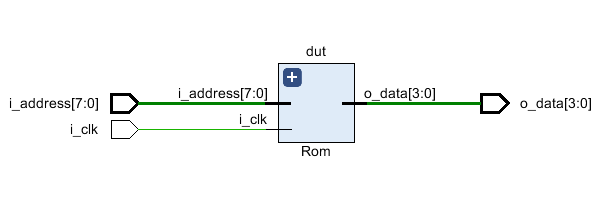


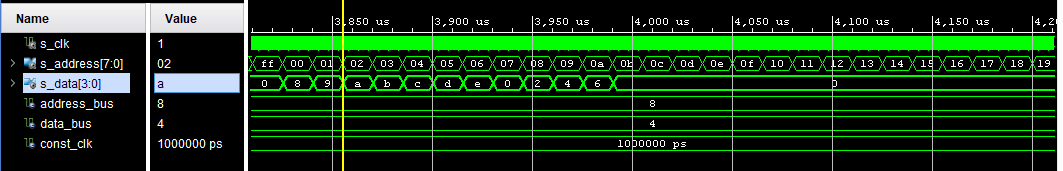
1. Ram



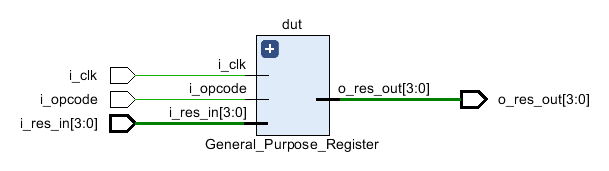


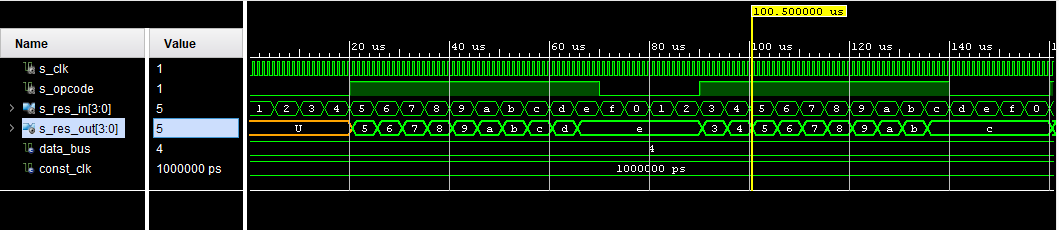
1. Rom



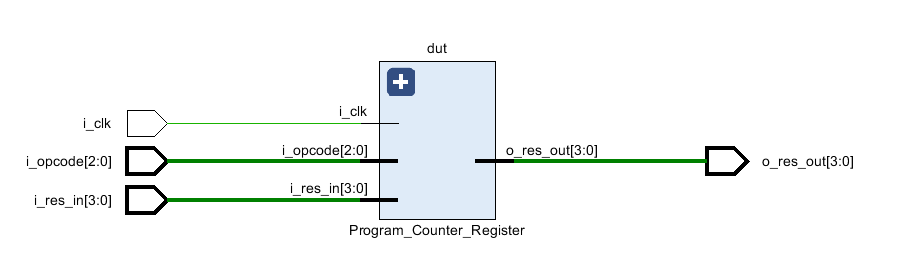


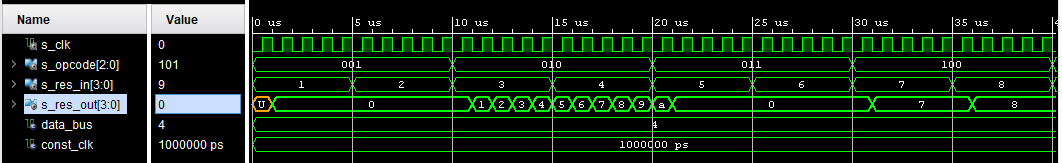
1. General Purpose Register



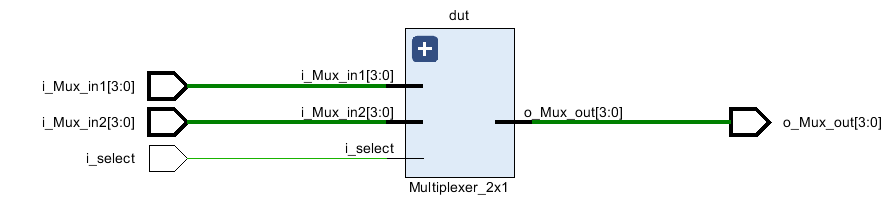


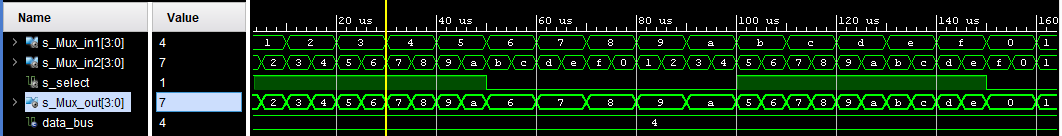
1. Program counter Register





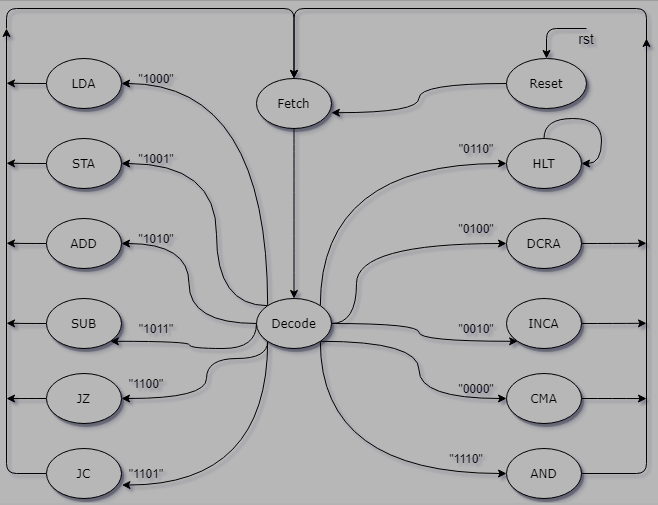
1. Multiplexer 2 to 1

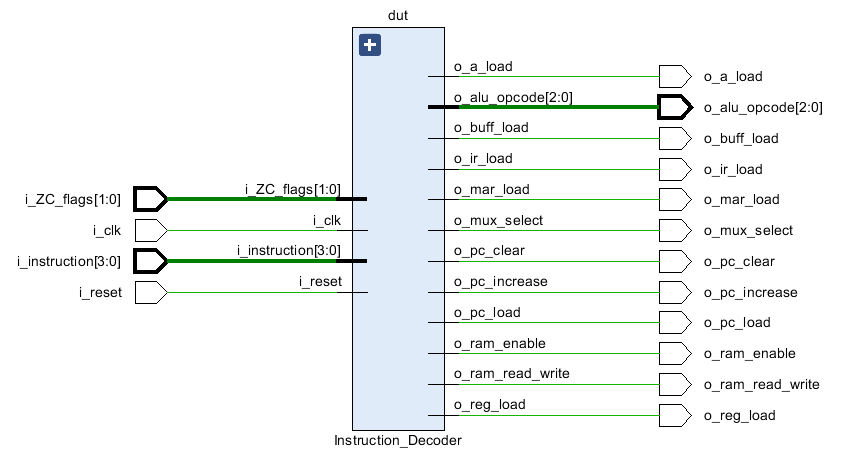


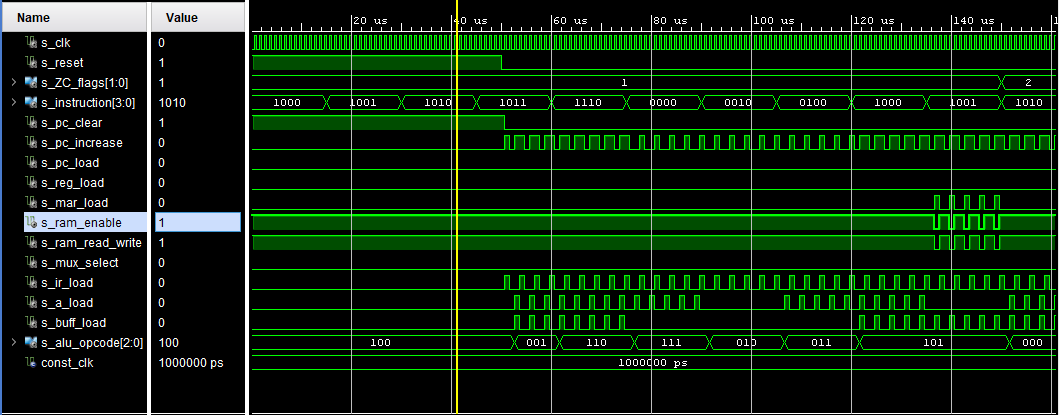


1. Instruction Decoder

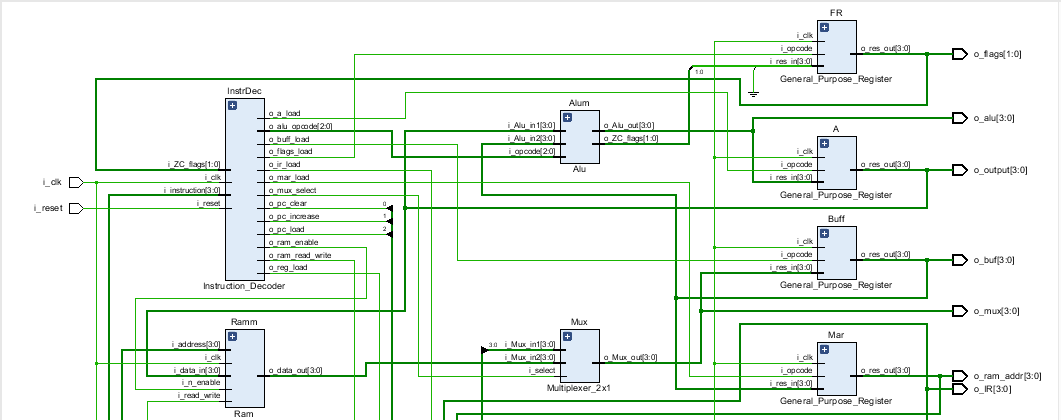
FSM:

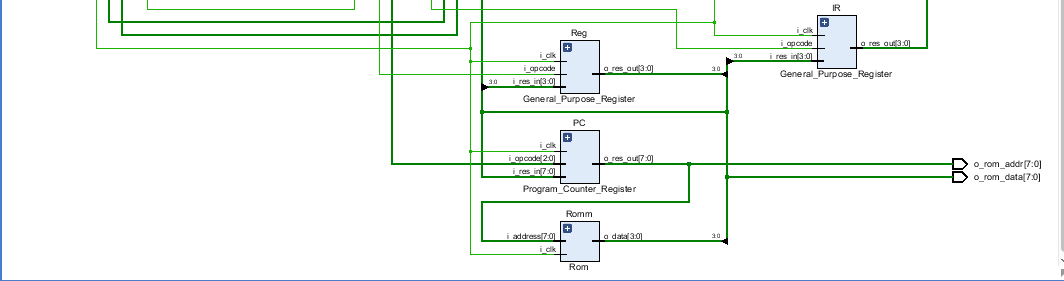


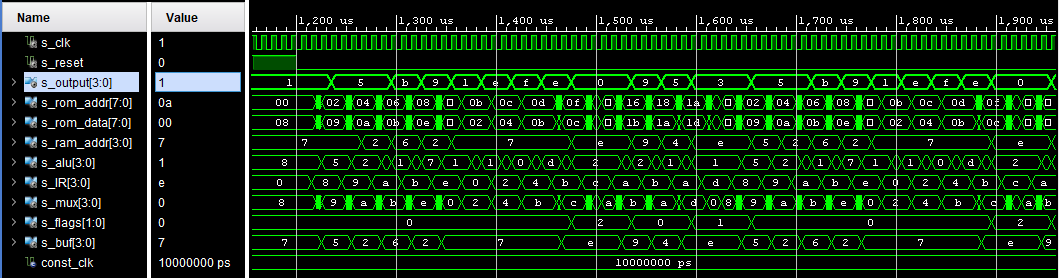


t

1. Microprocessor







* Program:

Memory Address Memory Data

lda A, #5 A <- #5 (5) 00h : 1000

01h : 0101

sta A, 2H 2H <- A (5) 02h : 1001

03h : 0010

add A, #6 A <- A + #6 (b) 04h : 1010

05h : 0110

sub A, #2 A <- A – #2 (9) 06h : 1011

07h : 0010

and A, #7 A <- A and #7 (1) 08h : 1110

09h : 0111

cma A A <- not A (e) 0ah : 0000

inca A A <- A + 1 (f) 0bh : 0010

dcra A A <- A – 1 (e) 0ch : 0100

sub A,#e A <- A – e (0) 0dh : 1011

0eh : 1110

jz #12h PC <- #14 0fh : 1100

10h : 0001

11h : 0100

add A, #8 A <- A + 8 (8) 12h : 1010

13h : 1000

add A, #9 A <- A + 9 (9) 14h : 1010

15h : 1001

sub A, #4 A <- A – 4 (5) 16h : 1011

17h : 0100

Add A, #14 A <- A + e(3) 18h : 1010

(C=1) 19h : 1110

Jc #00h PC <- #00h 20h : 1101

21h : 0000

22h : 0000

Hlt 23h : 0110